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	Application No.	Applicant(s)	
	09/837,995	MUKHERJEE ET AL.	
Notice of Allowability	Examiner	Art Unit	
	Anne L Damiano	2114	
The MAILING DATE of this communication appeals All claims being allowable, PROSECUTION ON THE MERITS IS herewith (or previously mailed), a Notice of Allowance (PTOL-85) NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT R of the Office or upon petition by the applicant. See 37 CFR 1.313	(OR REMAINS) CLOSED in this app or other appropriate communication IGHTS. This application is subject to	olication. If not include will be mailed in due	ed course. THIS
1. X This communication is responsive to <u>amendment filed 5/10/04</u> .			
2. The allowed claim(s) is/are <u>1-18</u> .			
3. 🔀 The drawings filed on <u>10 May 2004</u> are accepted by the Examiner.			
4.			
 Attachment(s) 1. ☑ Notice of References Cited (PTO-892) 2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948) 3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB, Paper No./Mail Date	Paper No./Mail Da /08), 7. ⊠ Examiner's Amend —	y (PTO-413), ate Iment/Comment	

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Mark E. Scott (Reg. # 43,100) on 9/30/04.

The application has been amended as follows:

Claim 5 (line 3) insert --only-- following "as between the at least two threads."

Claim 11 (line 4) replace "our" with --out-- following "thread to execute program steps."

Claim 13 (line 17) insert --only-- following "between the leading and trailing threads."

Allowable Subject Matter

2. Claims 1-18 are allowed.

The following is an examiner's statement of reasons for allowance:

The primary reason for allowance of claims 1-4 is the inclusion a store queue that stores memory requests that directly or indirectly change values in the system memory, a compare logic that scans the contents of the store queue for corresponding memory request matches, and based

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on whether the corresponding memory requests match, performs one of allowing the memory request to execute or initiating fault recovery, in a computer system comprising a pipelined, simultaneous and redundantly threaded processor having at least two threads as recited in the claims.

The primary reason for allowance of claims 5-7 is the inclusion of verifying, as between at least two threads, only committed store requests and data load requests from sources that are not cached in a method of checking for transient faults in a pipelined, simultaneous and redundantly threaded processor having at least two threads as recited in the claims.

The primary reason for allowance of claims 8-11 and claims 14-17 is the inclusion of executing programs as first and second threads, generating first and second committed store requests; checking an address and data associated with the first committed store request against an address and data associated with the second committed store request in a compare logic; and allowing one of the first and second commands to execute if the checking step shows those commands are the same in a method of detecting transient faults in a simultaneous and redundantly threaded microprocessor having at least two threads, as recited in the claims.

The primary reason for allowance of claims 12 and 18 is the inclusion of first and second pipelines executing first and second program threads that independently generate corresponding committed write requests, a store queue coupled to the first and second pipelines, a compare circuit coupled to the store queue, wherein each thread places the committed write requests in the

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store queue; and wherein the compare circuit detects transient faults in operation of the first and second pipeline by comparing the committed store requests from each thread, in a simultaneous and redundantly threaded microprocessor as recited in the claims.

The primary reason for allowance of claim 13 is the inclusion of the processor that processes instructions in leading and trailing threads and wherein the processor detects transient faults by verifying as between the leading and trailing threads only the committed stored and uncached memory read requests, in a pipelined, simultaneous and redundantly threaded processor as recited in the claim.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anne L Damiano whose telephone number is (703) 305-8010. After approximately October 13th, the examiner can be reached at (571) 272-3658. The examiner can normally be reached on M-F 9-6:30 first Fridays off.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (703) 305-9713. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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ROBERT BEAUSOLIEL
SUPERVISORY PATENT EXAMINER

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